Front-End Data Acquisition and Signal Processing for the ADAPT Telescope

High-Throughput, Low-Latency FPGA-Based Preprocessing to Enable Multi-Messenger Transient Observations

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APT [1,2]

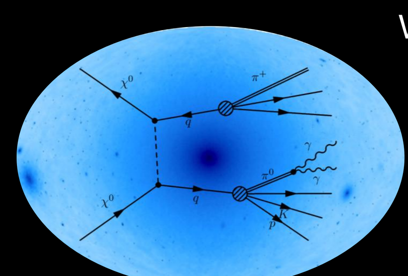
The Advanced Particle-astrophysics Telescope (APT)

Proposed gamma-ray/cosmic-ray mission

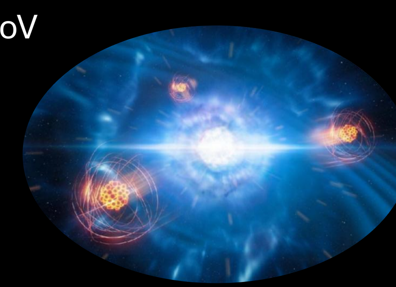
Larger effective area, better sensitivity than Fermi

Will fly at L_2 for full-sky FoV

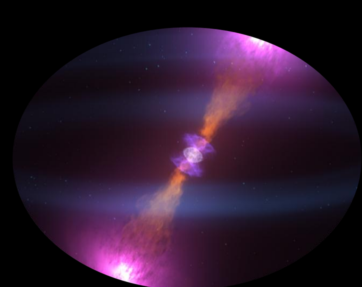
(See James Buckley's poster, "The ADAPT Mission")



Constrain thermal WIMP dark matter



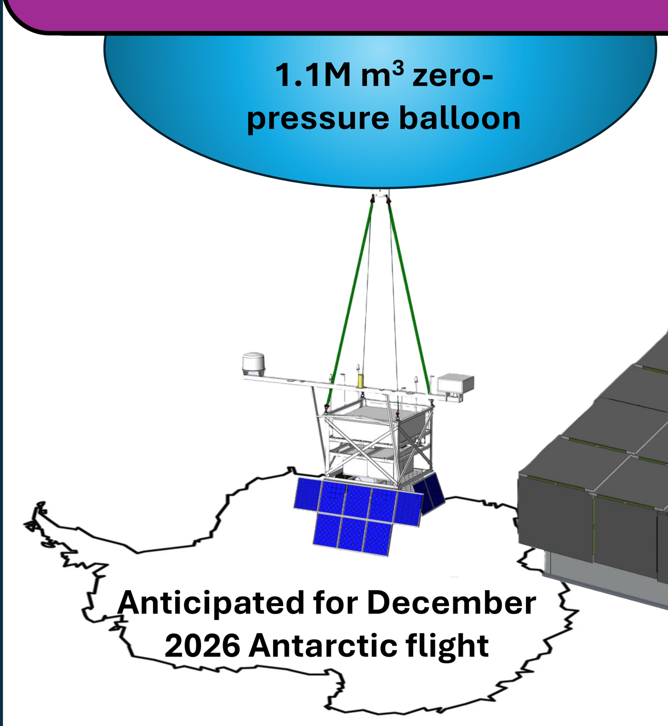
Probe origin of the heavy elements



Perform onboard, real-time Compton reconstruction and localization to enable rapid multi-messenger follow-up observations [4-9]

(See Ye Htet's poster, "Neural Network Extensions for the GRB Localization Pipeline on the ADAPT Gamma-Ray Telescope")

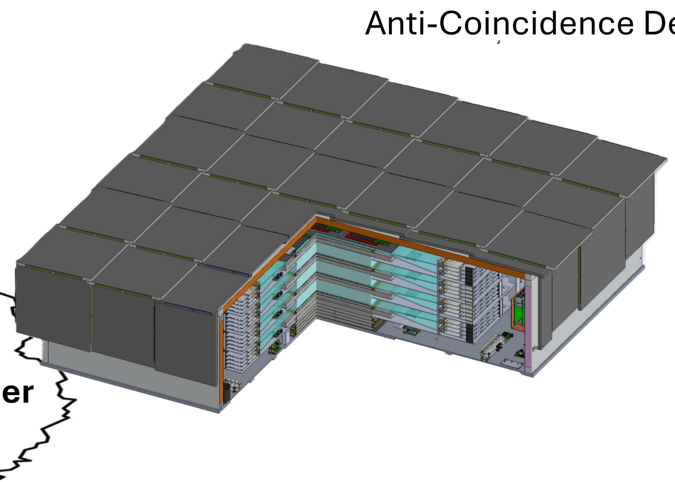
ADAPT [3]

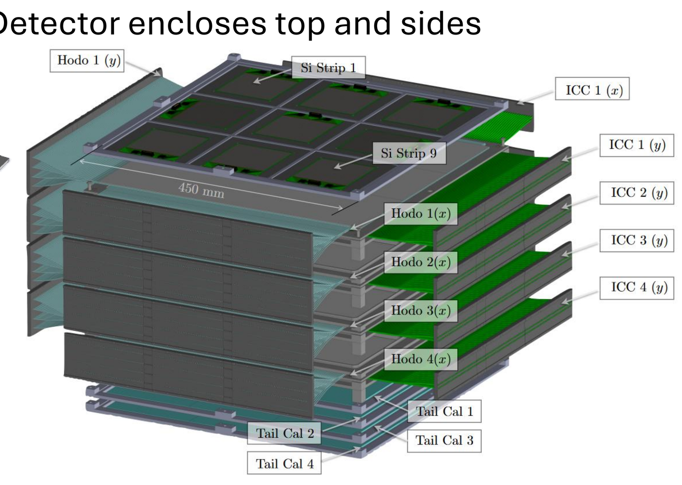


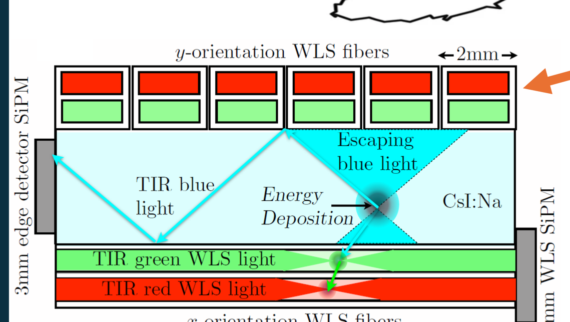
The Antarctic Demonstrator for APT (ADAPT)

0.45m x 0.45m cross-sectional area partially covered at top with a layer of Silicon Strip Detectors (SSD)

Anti-Coincidence Detector encloses top and sides





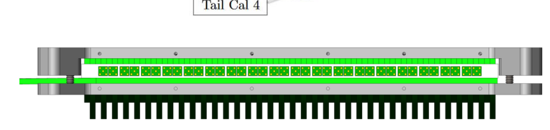


4 layers of CsI:Na imaging calorimeter (ICC) detectors

4 layers of scintillating fiber tracker (hodoscope)

4-layer tail counter calorimeters

WLS and tracker fiber SiPMs shaped by SMART preamplifier ASIC [10]

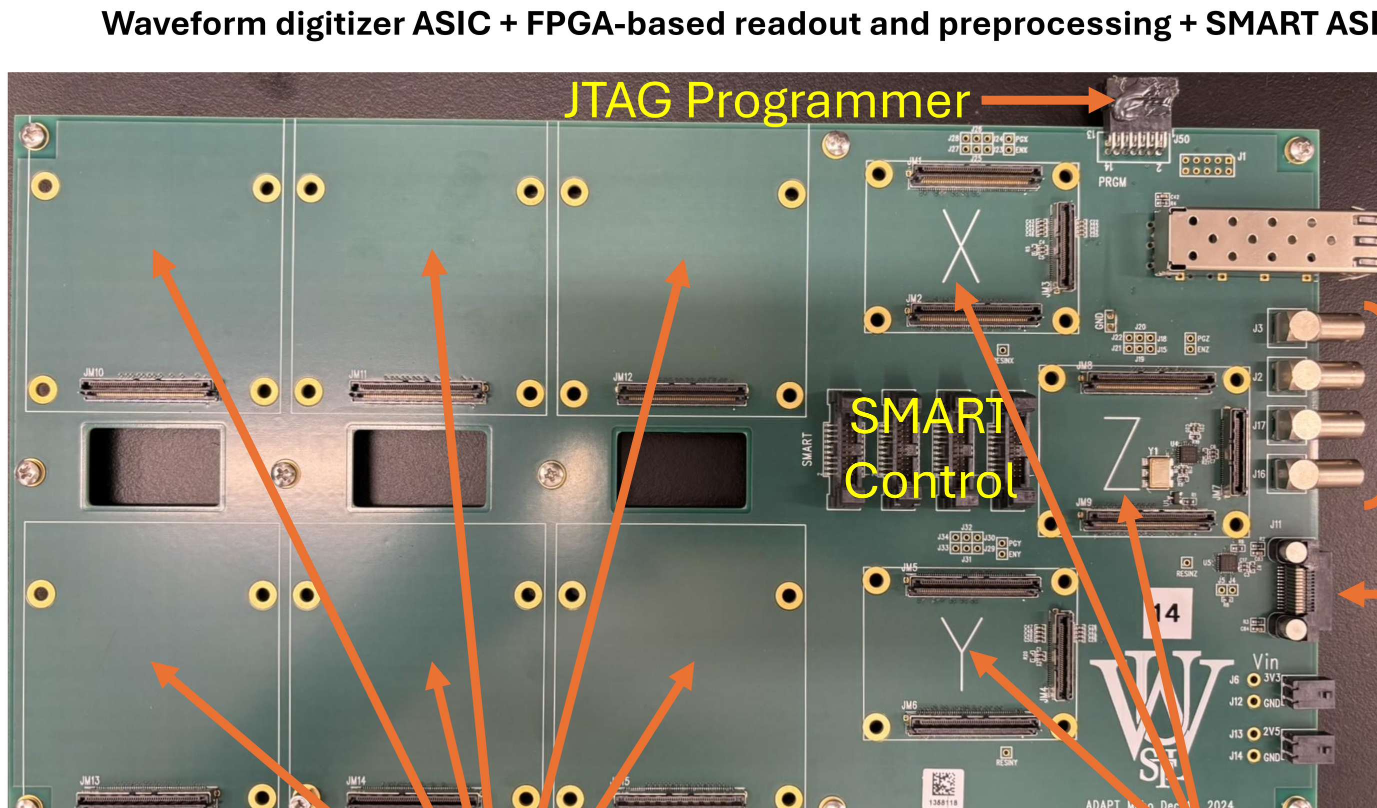


Edge detector SiPMs on ICC and tail counters passively combined into low- and high-gain preamplifier stages

SMART ASIC and preamplifiers read out by waveform digitizer ASICs

13x ADAPT Data Acquisition Motherboard

Waveform digitizer ASIC + FPGA-based readout and preprocessing + SMART ASIC control + Triggering

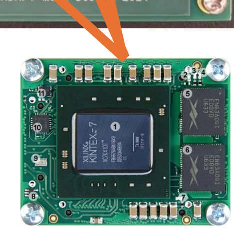


SFP module with RJ45 PHY (1 GbE)

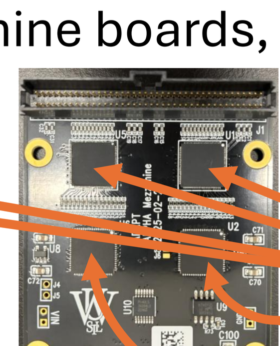
LEMO Debug Points (e.g., for external trigger in lab tests)

To Trigger Board

(Actual Size)



Slots for 6 ASIC mezzanine boards, either:



Slots for 3 FPGA SoMs

- Trenz TE0741 module
- AMD/Xilinx Kintex-7 325T FPGA

CT5TEA Trigger ASIC [11]

- 16 channels
- DAC supplies per-channel tunable pedestal voltage
- 4x 4-channel analog sum fed to tunable comparator for trigger logic
- 16-channel analog sum trigger logic

HDSoC Daughter Card

ALPHA Daughter Card

HDSoC ASIC

- 32-channel waveform digitizer ASIC
- Made by Nalu Scientific
- 1 Gsps or 250 Msps sampling
- 1984-sample analog memory depth
- See Aera Jung's poster, "Evaluation of HDSoC ASIC"

ALPHA ASIC

- 16-channel waveform digitizer ASIC [12]
- Made by Gary Varner Lab at University of Hawaiʻi
- Based on Gary Varner's TARGET family ASIC design
- 100 or 250Msps Gsps or 250Msps sampling
- 2-bank, 256-sample analog memory depth

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FPGA Data Processing and Reduction [13,14]

Motivation

ADAPT's 13 motherboards support ~20Gbps sustained readout

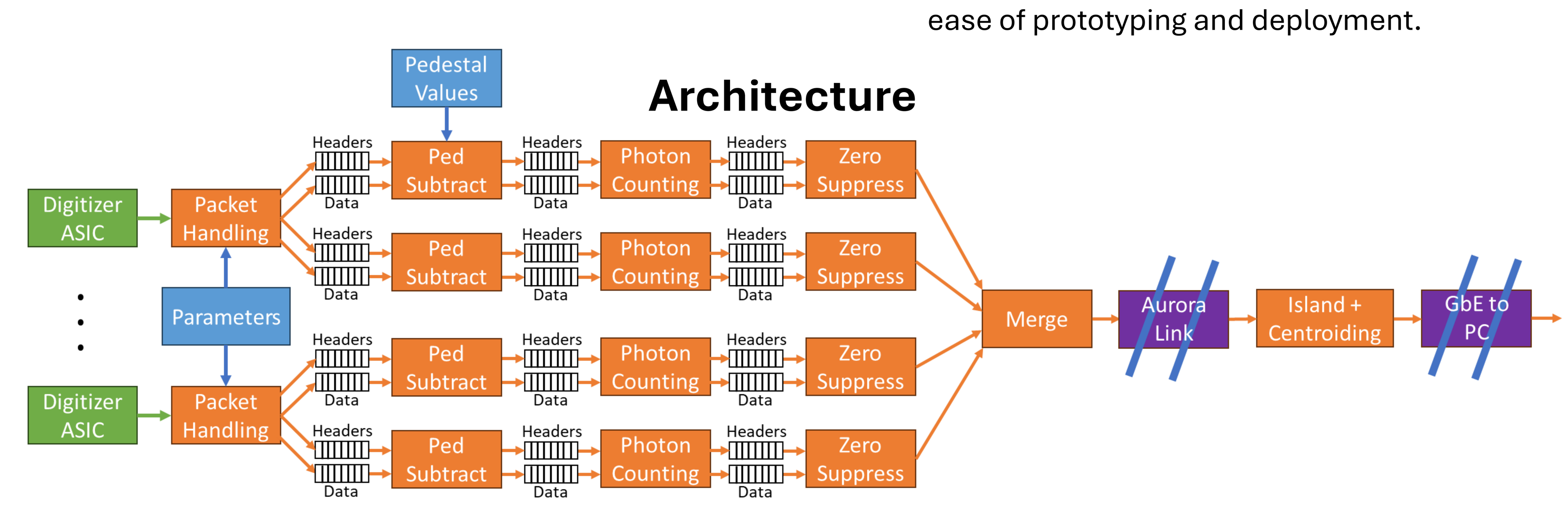
FPGAs process and reduce data for efficient back-end data storage and real-time Compton reconstruction and localization

HLS

Individual preprocessing algorithms are developed using **high-level synthesis** (HLS), allowing expression using high-level languages (e.g., C/C++) instead of traditional hardware description languages (HDL) such as VHDL or Verilog, while supporting integration into the larger system architecture based on those languages.

With proper architecture and pragma selection, these provide high performance while providing benefits in ease of prototyping and deployment.

Architecture



Vector operations and dataflow pipeline architecture allow efficient streaming with high throughput

Packet Handling

- Read and deserialize digital packets from ASIC
- Push 16-channel vectorized data and preprocessing parameters into FIFO (`hls::stream`) for next stage

Pedestal Subtraction

- Subtract CT5TEA DAC voltage and capacitive charge pedestal from digitized samples
- Requires logical (w.r.t. trigger) to physical (w.r.t. analog memory) address translation

```
void ped_subtract(hls::stream<Header> & headers_in,
                  hls::stream<Header> & headers_out,
                  hls::stream<vec_uint16_16> & samples_in,
                  hls::stream<vec_int32_16> & ped_sub_results) {
    #pragma HLS bind_storage variable=peds type=RAM_1P impl=BRAM

    Header header = headers_in.read();
    headers_out << header;

    ped_samples: for (uint16_t s = 0; s < NUM_SAMPLES; ++s) {
        vec_uint16_16 svec = samples_in.read();
        // calculate base address
        const uint16_t idx = (header.starting_sample_number + s) % NUM_SAMPLES;
        vec_int32_16 rvec;
        ped_channel: for (uint8_t c = 0; c < NUM_CHANNELS; ++c) {
            uint16_t sval = svec[c];
            int32_t pval = peds[header.bank * NUM_SAMPLES + idx][c];
            int32_t rval = (int32_t) sval - (int32_t) pval;
            rvec[c] = rval;
        }
        ped_sub_results << rvec;
    }
}
```

Photon Counting

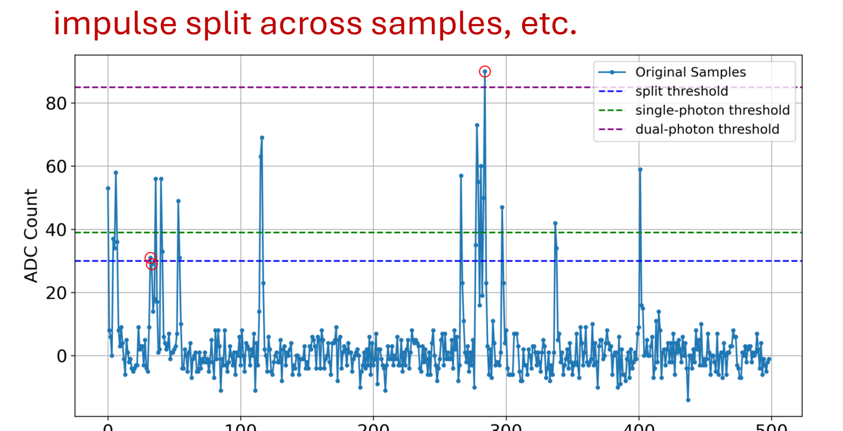
3 options

1. Waveform Integration

- Integrate a portion of the captured waveform
- Can efficiently integrate over multiple portions of waveform:
  - Prefix sum
  - Parallel circuits with loop unrolling `#pragma HLS UNROLL factor=num_integrals`
- Divide by area of single-PE impulse response
- For sparse PE signals in WLS fibers at Compton regime, integral captures a large amount of noise

2. Threshold-Based Analysis

- Count PE impulses based on samples above threshold
- Does not capture noise in signal-less regions
- Tuning thresholds is difficult
- Requires multiple thresholds to capture pileup, impulse split across samples, etc.



3. Hybrid Approach

- Use single threshold to identify likely PE
- Integrate in configurable window around any samples exceeding threshold
- Less tuning required
- Scales well to higher energy regimes

Zero-Suppression

- Integrals or PE counts under a configurable threshold treated as noise, set to 0.

Merge

- Loops over 16-channel vectorized PE values from upstream ASIC streams
- Produces single 80-channel vector for downstream processing

Aurora Link

- Data sent from X and Y FPGAs to Z FPGA for final aggregation and communication to PC via GbE
- Uses AMD/Xilinx Aurora protocol LogiCORE IP

Island Detection and Centroiding

- Determines position and intensity of each particle interaction within the detector
- Performs single scan over 80-channel array
- Track whether currently in an "island" of adjacent non-zero channels
- Registers track island's starting channel index, width, total intensity
- Multiply-accumulate circuit computes intensity-weighted position
- Divide at end to get interaction position

Performance Results

Achievable Throughput

- Events are individual gamma-ray detections
- Pipeline performance is governed by slowest stage
- Currently bottlenecked by digitizer ASIC serial outputs

Module	Throughput
Ped Subtract	383 000 events/s
Photon Counting (Integral)	369 000 events/s
Photon Counting (Threshold)	381 000 events/s
Photon Counting (Hybrid)	64 000 events/s
Zero Suppress	4 350 000 events/s
Island + Centroiding	446 000 events/s

Resource Usage

- Counts:16 channels, Percentage: 80 channels

Module	LUTs	FFs
Packet Handling (5x)	8 820 (22%)	751 (0.9%)
Ped Subtract (5x)	785 (1.9%)	558 (0.7%)
Photon Counting: Hybrid (5x)	4 813 (12%)	3 671 (4.5%)
Zero Suppress (5x)	9 263 (23%)	2 115 (2.6%)
Island + Centroiding (1x)	36 671 (18%)	46 483 (11%)

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[3] Chen et al. "Simulation of the instrument performance of the Antarctic Demonstrator for the Advanced Particle-astrophysics Telescope in the presence of the MeV background." ICRC 2023.
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